REMARKS

Claims 21-48 are pending in the application. By this paper, independent claims 21, 38 and 48 have been amended. Reconsideration and allowance of claim 21-48 are respectfully requested.

Prior Art Rejection

Claims 21 and 23-48 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. patent number 6,297,524 to Vathulya, et al. ("Vathulya"). Claim 22 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Vathulya. Reconsideration of these rejections is respectfully requested.

Claim Amendments

Claim 21 has been amended to further clarify the features that distinguish this invention over Vathulya. Claim 21 recites a semiconductor component having first and second capacitance surface parts. The second capacitance surface part is in the form of a homogeneous cohesive elevation. The current amendment clarifies that the elevation comprises **a top wall and side walls** which are **covered by the insulating layer**. The top wall is oriented perpendicular to the side walls. Support for this amendment may be found in FIG. 1 of the application and the text associated therewith. For example, elevation 1f illustrated in FIG. 1 clearly shows elevation 1f having the form of a bar and arranged at a right angle to plate 1. Other bars-like regions 1a-1j are similar. Each has side walls (four side walls in the exemplary illustration of FIG. 1), the side walls terminating in a top wall. The side walls are perpendicular to the plate 1 and the top wall is substantially perpendicular to the side walls. As is further shown in, for example, FIG. 1, the top wall and the side walls extend into the insulating layer between the first metallization plane and the second metallization plane. The top wall and side walls are therefore covered by the insulating layer.

The Final Office Action notes that the elevation portion 32 of Vathulya "is surrounded on the left side and the right side by the insulating layer (27-30)" (page 3, lines 6-8). The elevation

portions 32 are actually electrically conductive vias extending through dielectric layers 26, 27, 28, 29. The vias 32, however, are continuous and electrically engage the adjacent electrically conductive lines 22, 23, 24, 25. Thus, the vias 32 of Vathulya do not have a top wall and side walls which are covered by the insulating layer as recited in claim 21. Since Vathulya's vias extend all the way to the adjacent electrically conductive line, they do not have a top wall. There is no showing or description of side walls for the vias 32. Accordingly, it is submitted that claim 21 recites limitations nowhere shown, described or suggested in Vathulya or any of the prior art of record.

Claims 38 and 48 have been similarly amended to further clarify the features of this invention over the disclosure of Vathulya. Accordingly, each of amended independent claims 21, 38 and 48 recites limitations nowhere shown, described or suggested by Vathulya. It is therefore submitted that the invention defined by these claims is patentable over this reference. The claims dependent on each of independent claims 21, 38 and 48 add further limitations to their respective independent claims and are allowable for at least the same reasons. Withdrawal of the rejection of claims 21-48 is therefore respectfully requested.

With this response, the application is believed to be in condition for allowance. Should the examiner deem a telephone conference to be of assistance in advancing the application to allowance, the examiner is invited to call the undersigned attorney at the telephone number below.

Respectfully submitted,

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